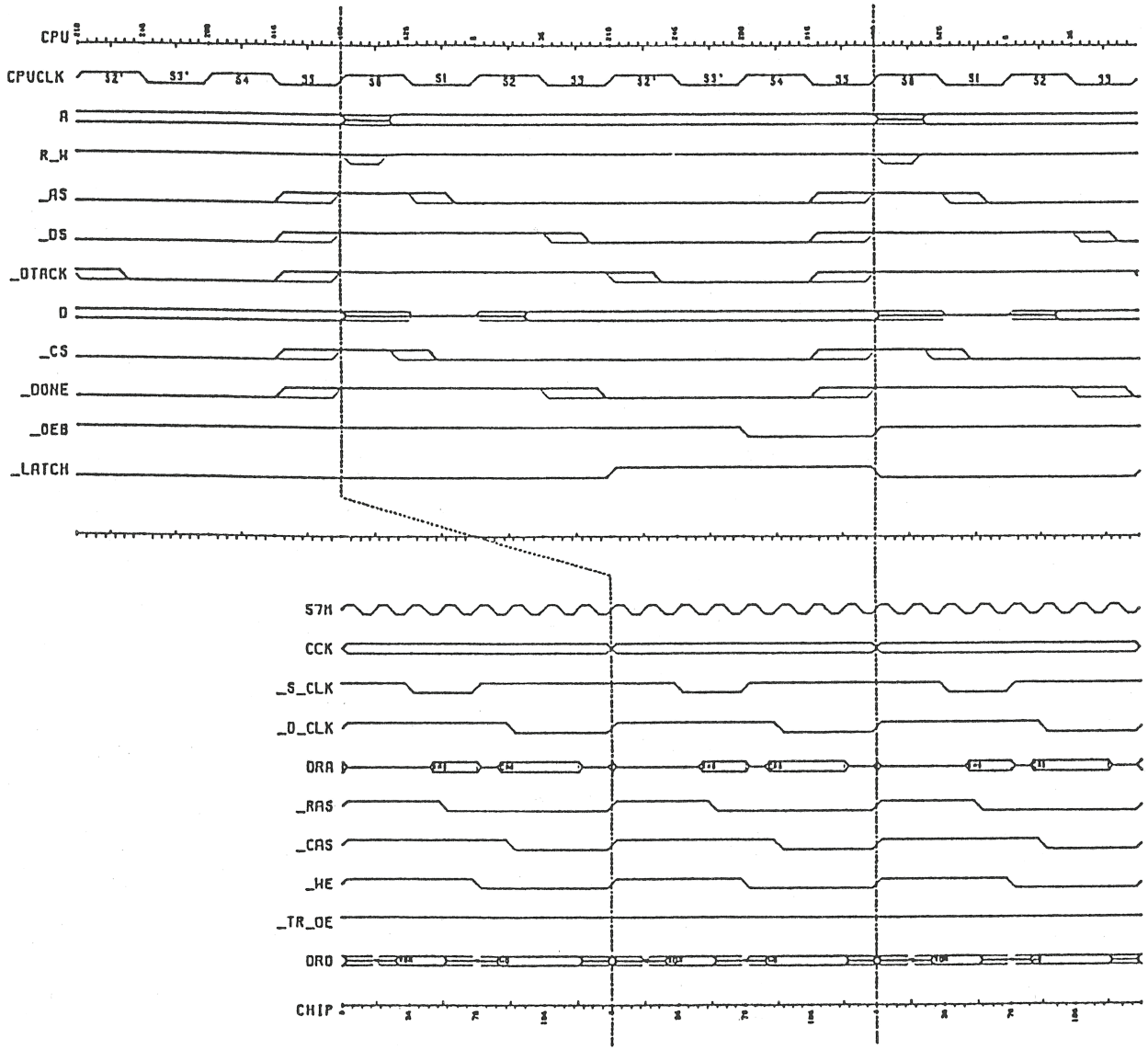
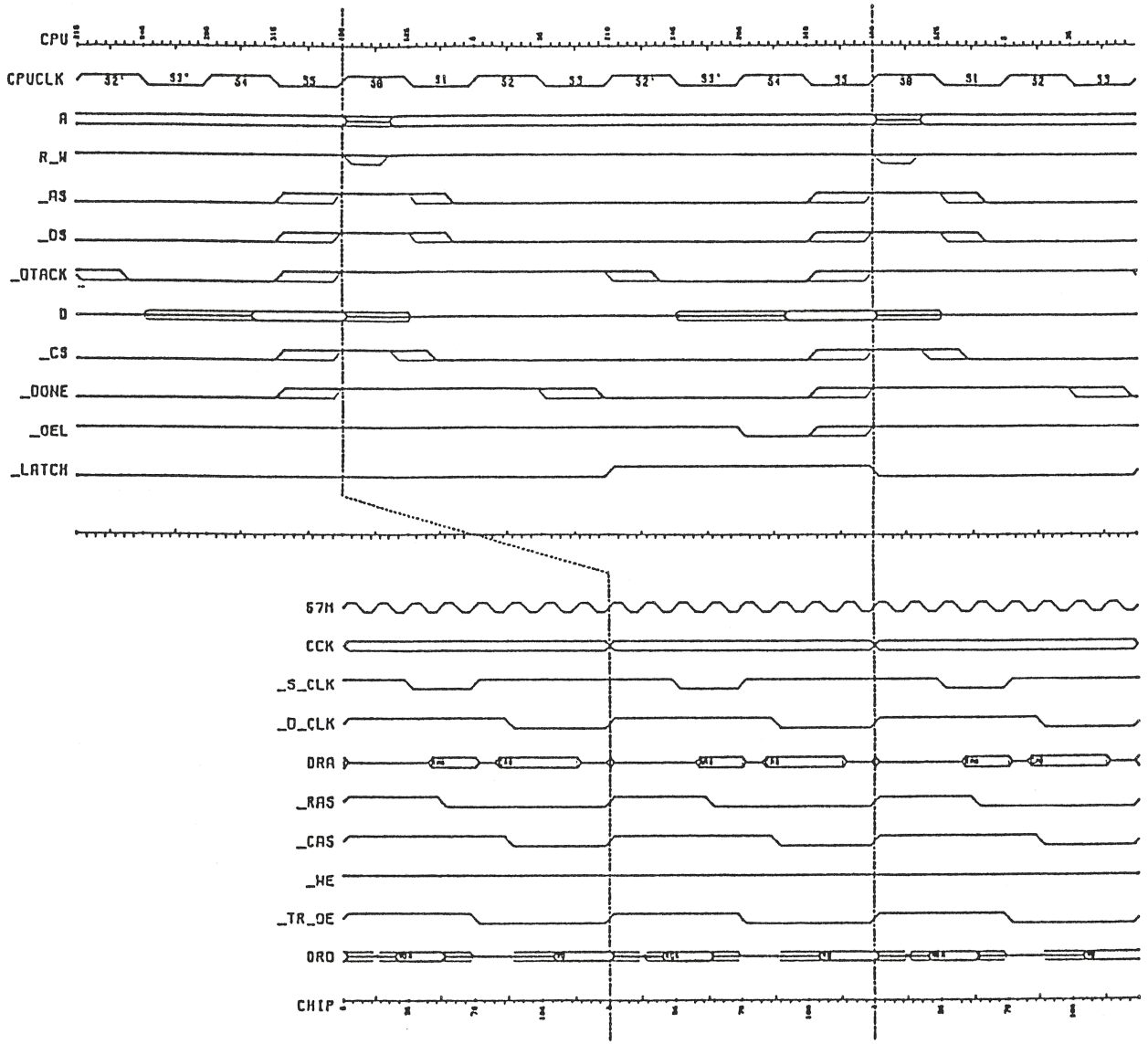


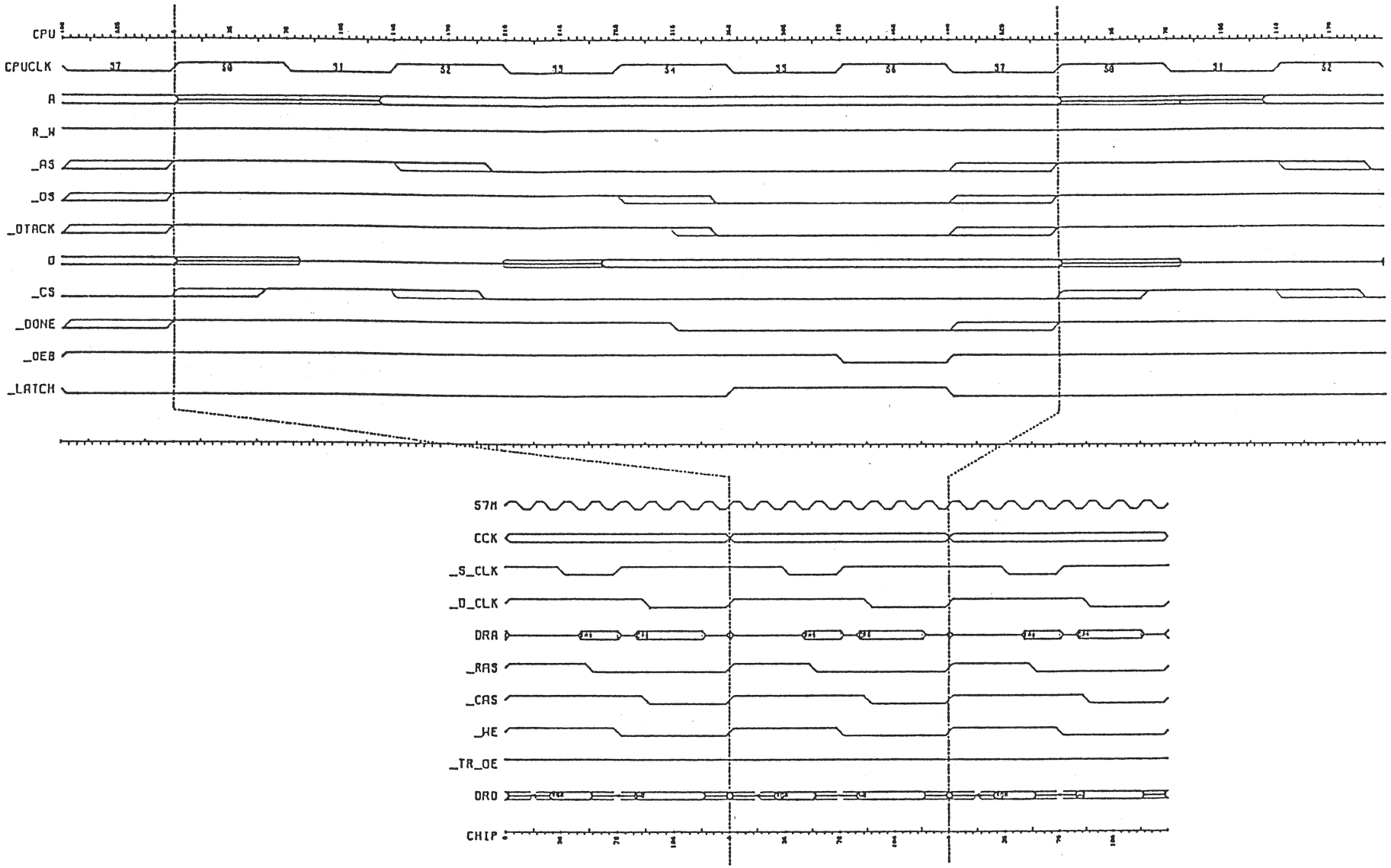
PROCESSOR WRITE CYCLE (14 MHz 68020/030)

A+ Processor/Chip Bus Timing Relations 04/01/92



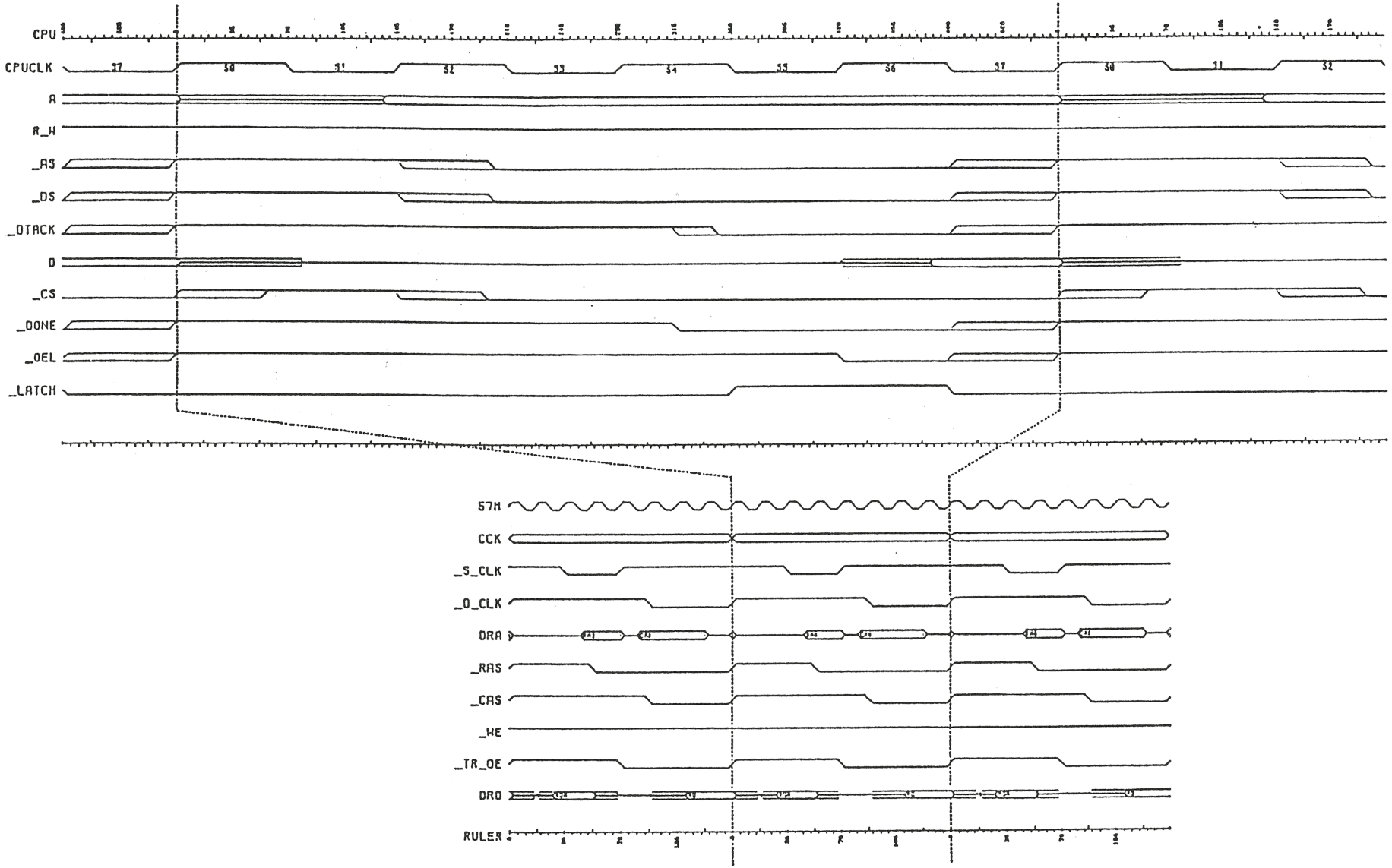
PROCESSOR READ CYCLE (14 MHZ 68020/030)

A+ Processor/Chip Bus Timing Relations 04/01/92



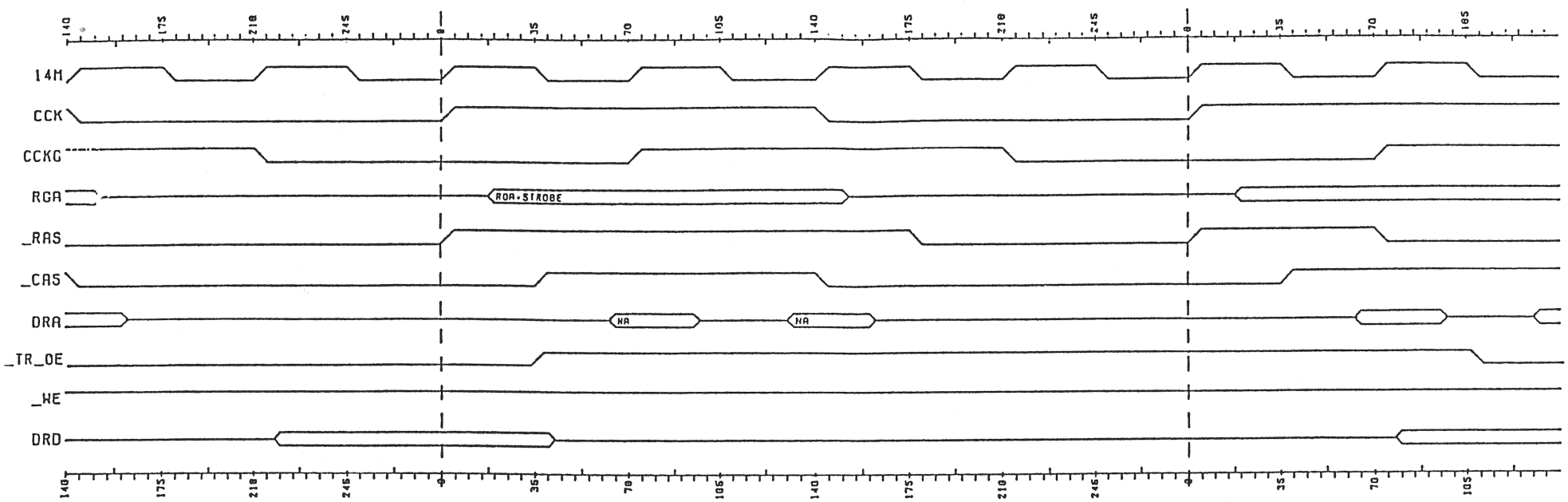
PROCESSOR WRITE CYCLE (7MHz 68000)

A+ Processor/Chip Bus Timing Relations 04/01/92

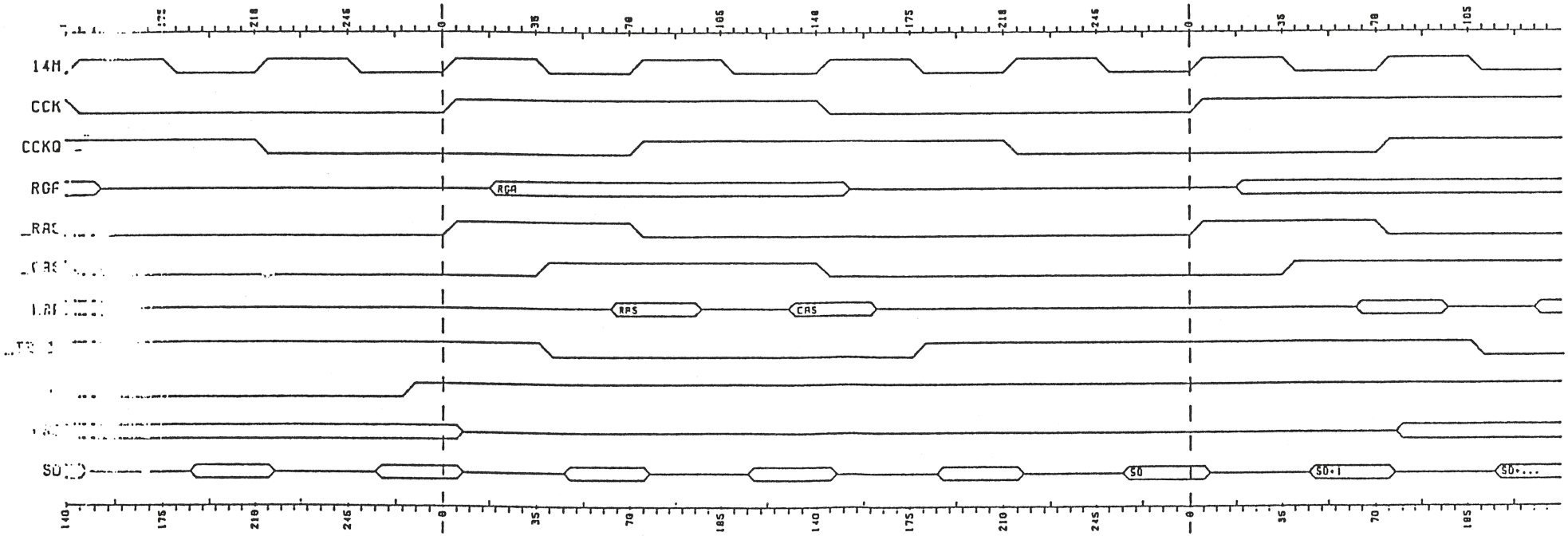


PROCESSSOR READ CYCLE (7MHz 68000)

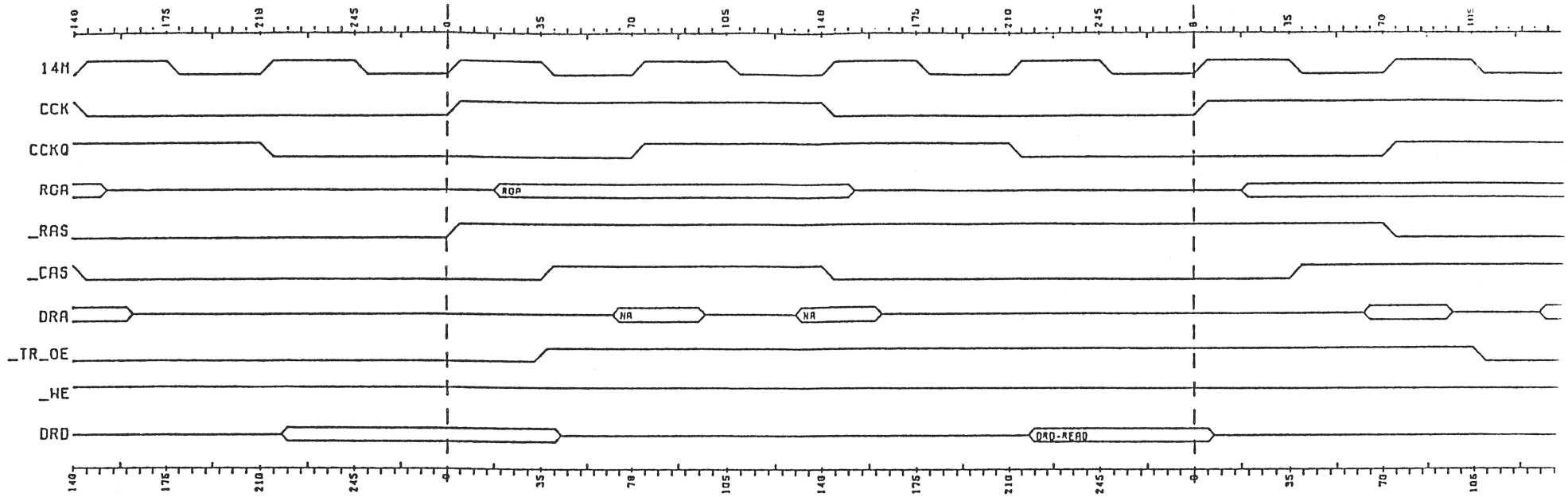
A+ Processor/Chip Bus Timing Relations 04/01/92



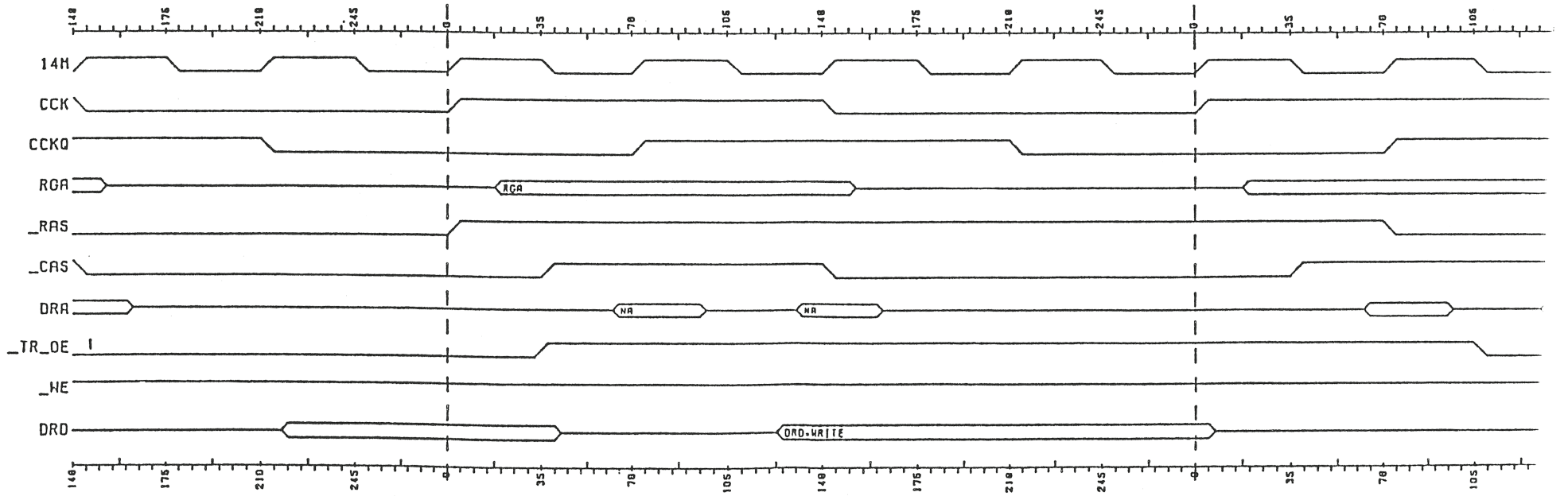
NEW CAS BEFORE RAS REFRESH



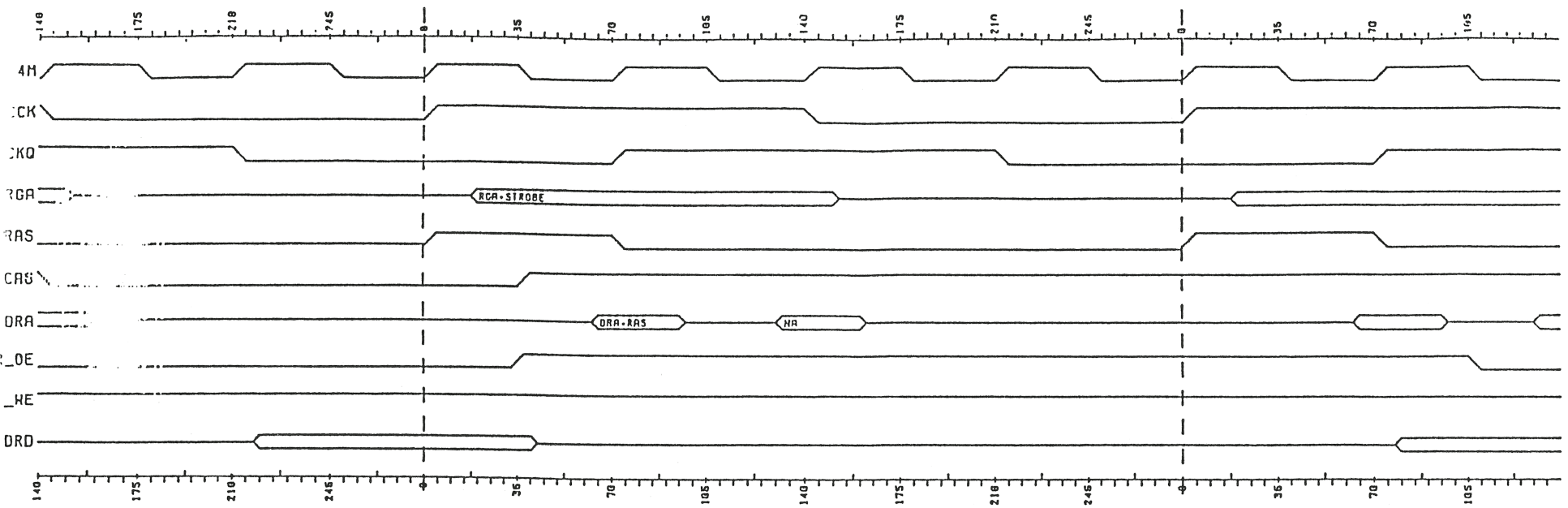
NEW SHIFT REGISTER LOAD CYCLE



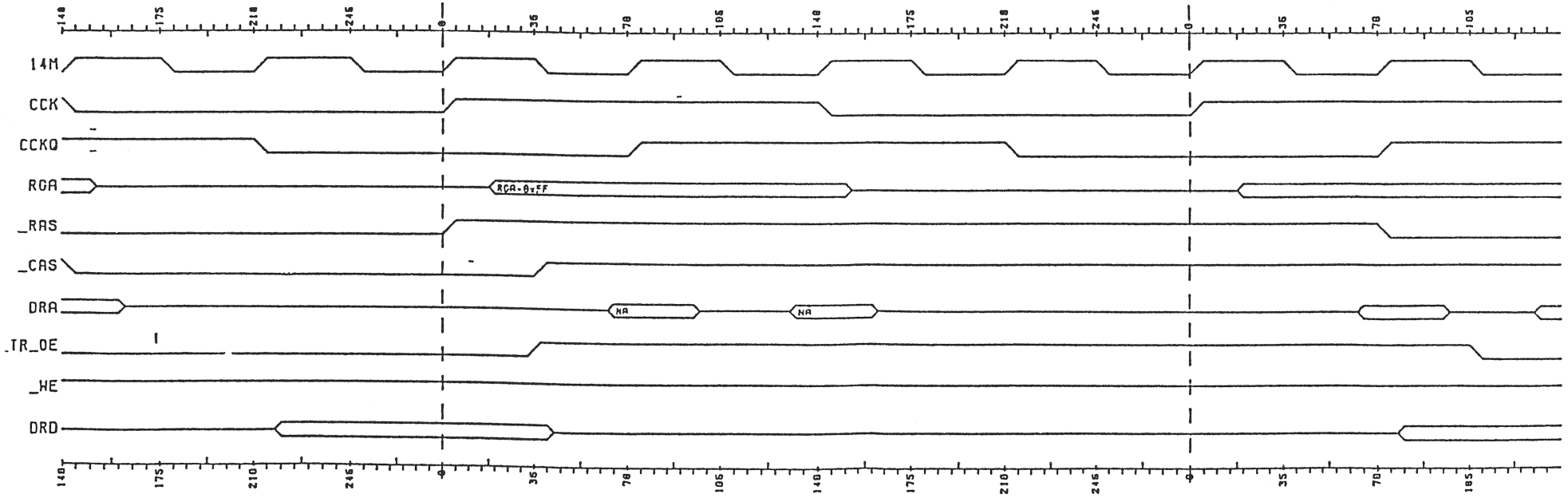
REVISED REGISTER READ CYCLE



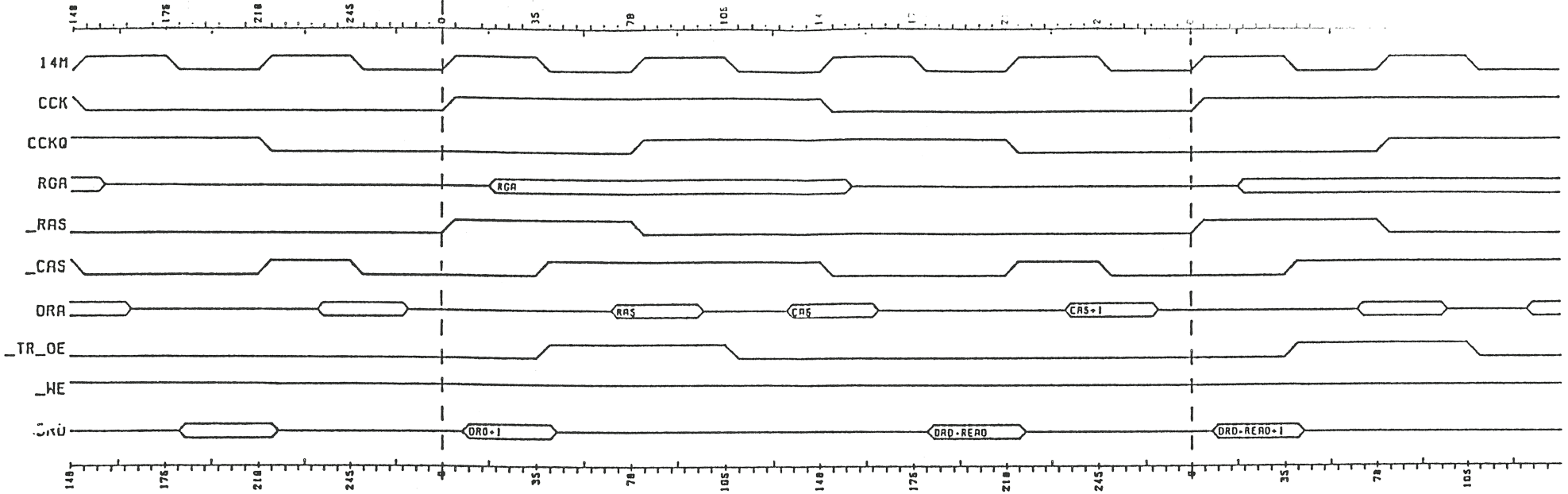
REVISED REGISTER WRITE CYCLE



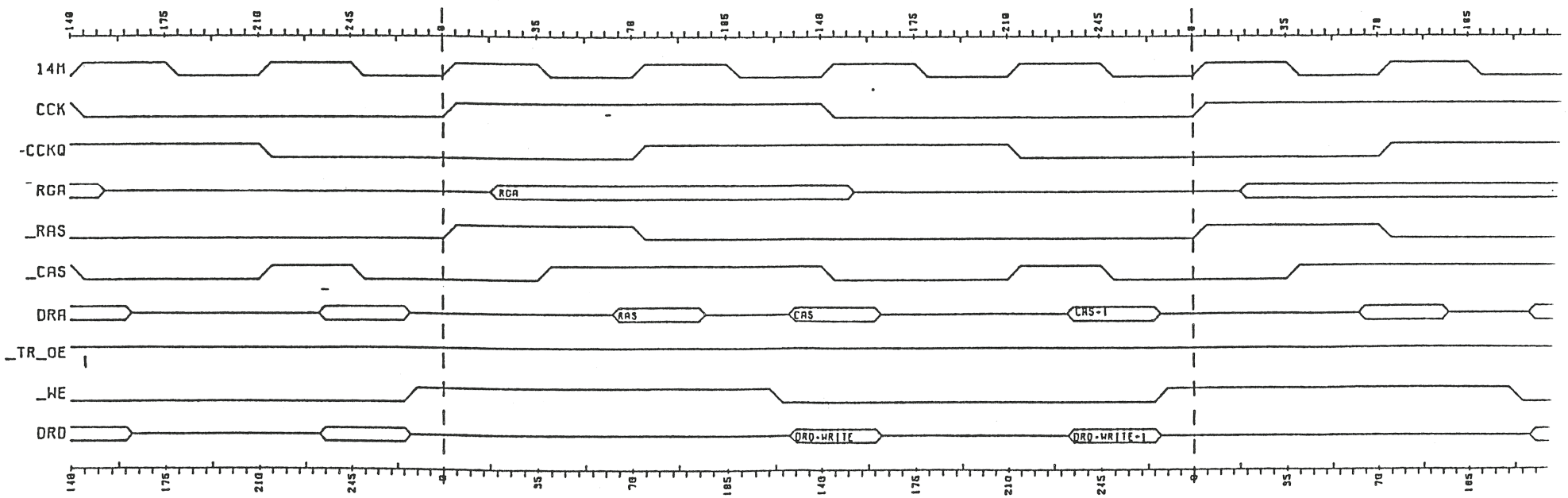
REVISED RAS ONLY REFRESH



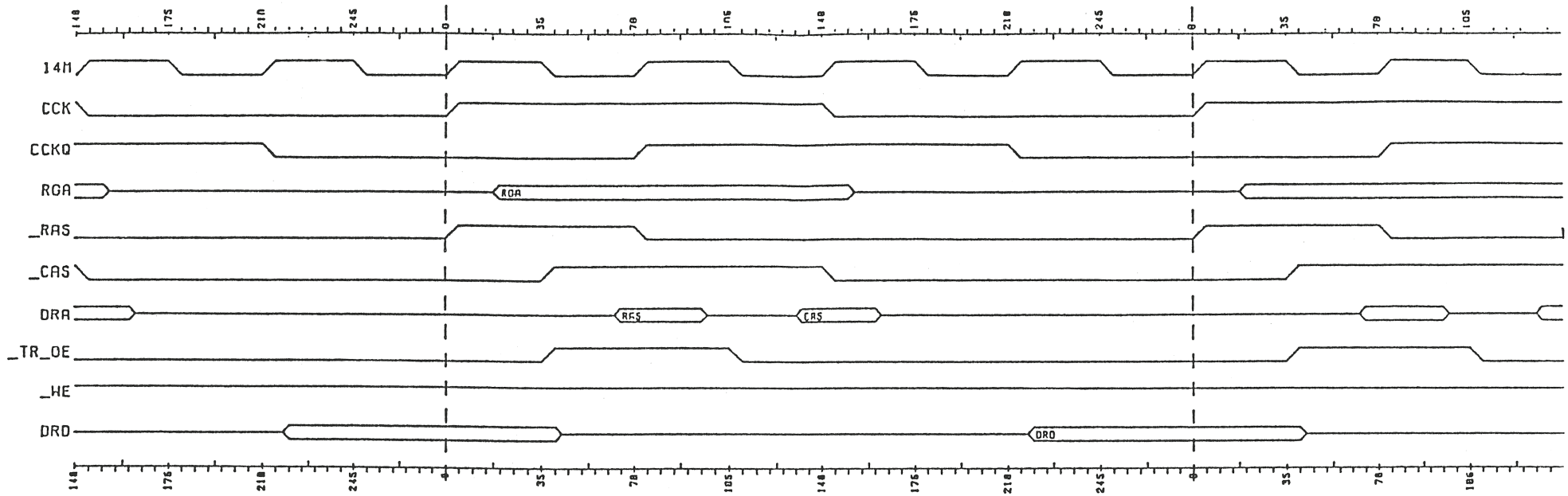
REVISED NULL CYCLE



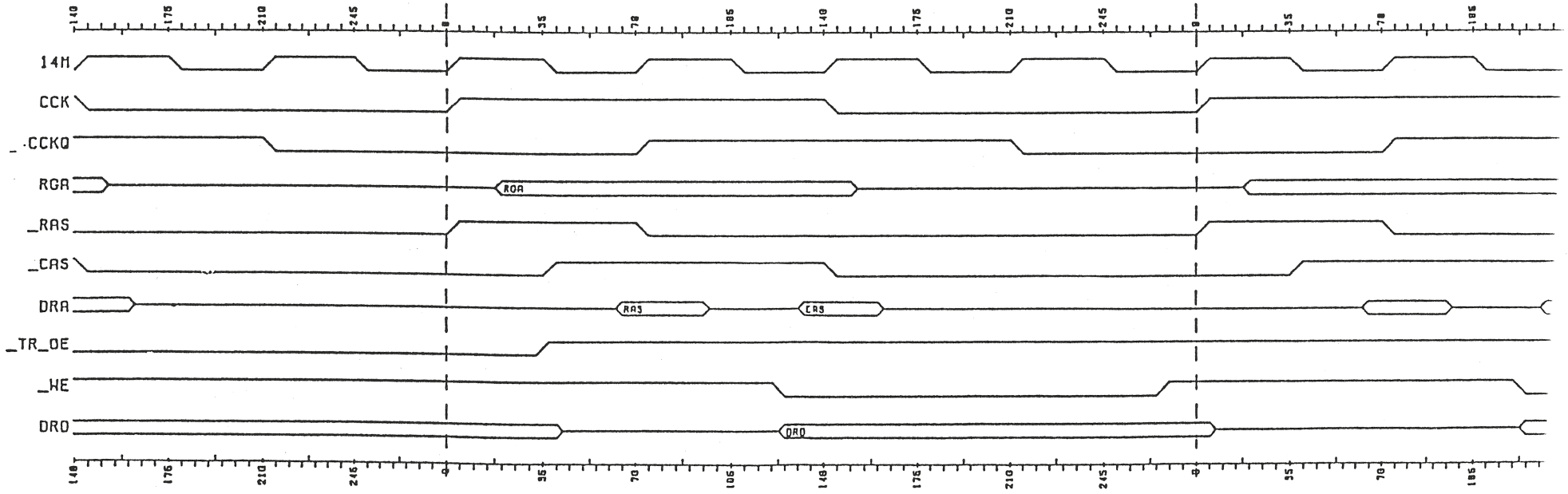
PAGE MODE DRAM READ CYCLE



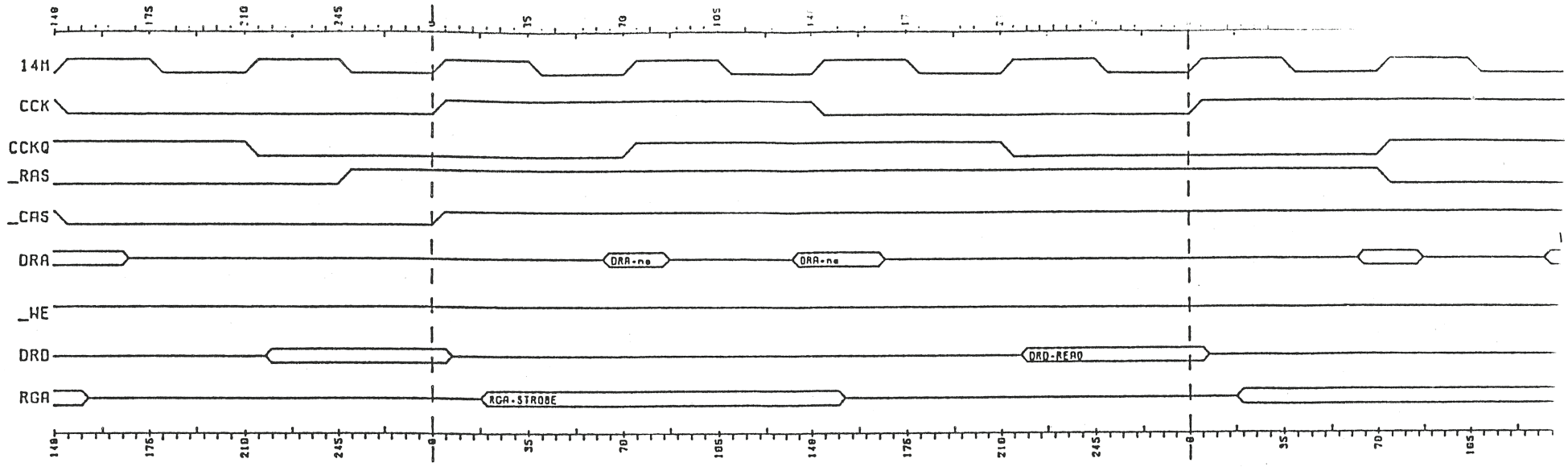
PAGE MODE DRAM WRITE CYCLE



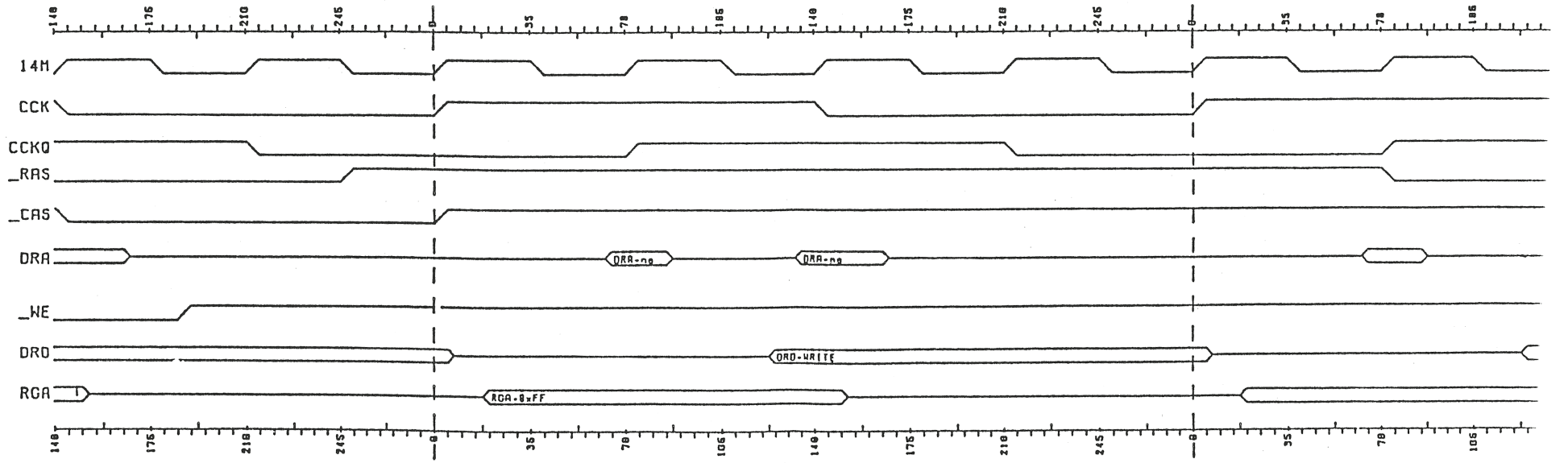
REVISED DRAM READ CYCLE



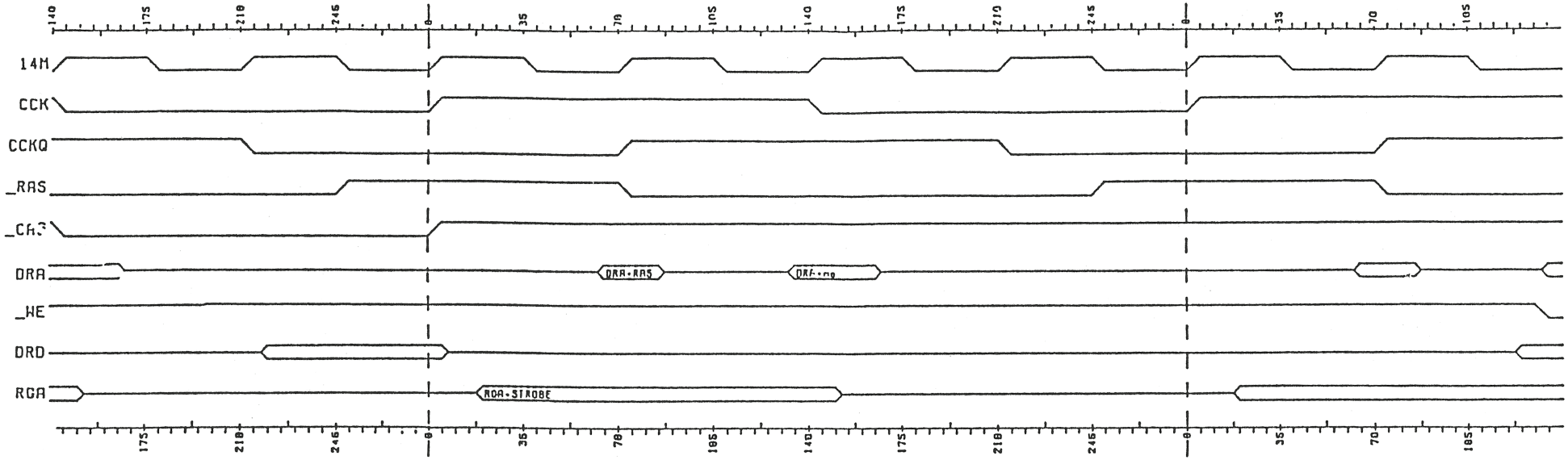
REVISED DRAM WRITE CYCLE



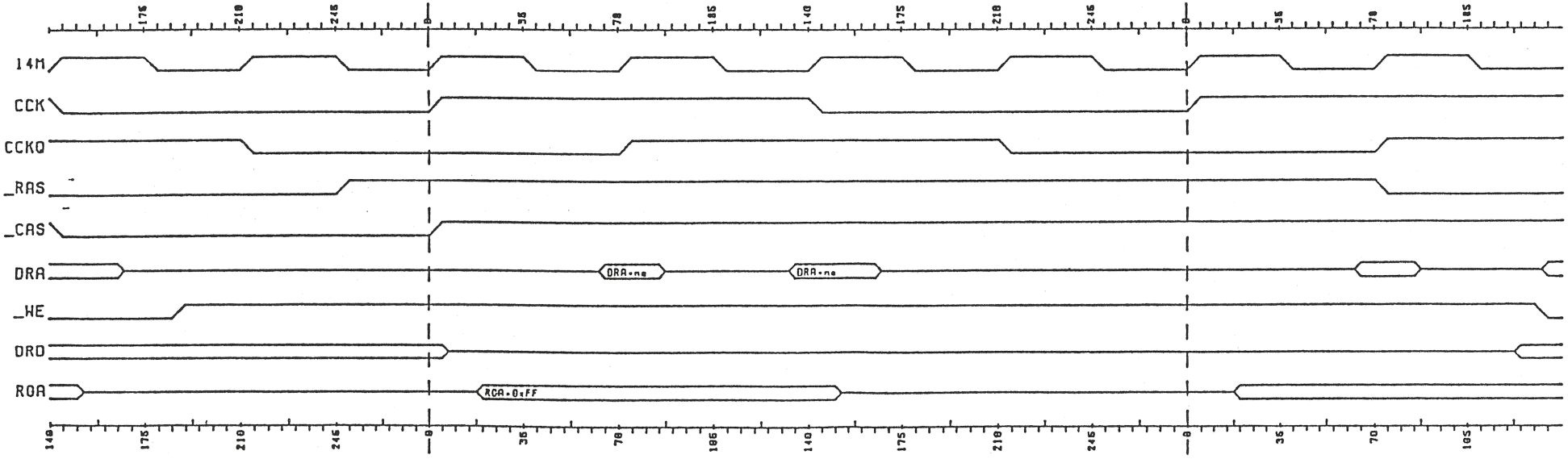
TRADITIONAL REGISTER READ CYCLE



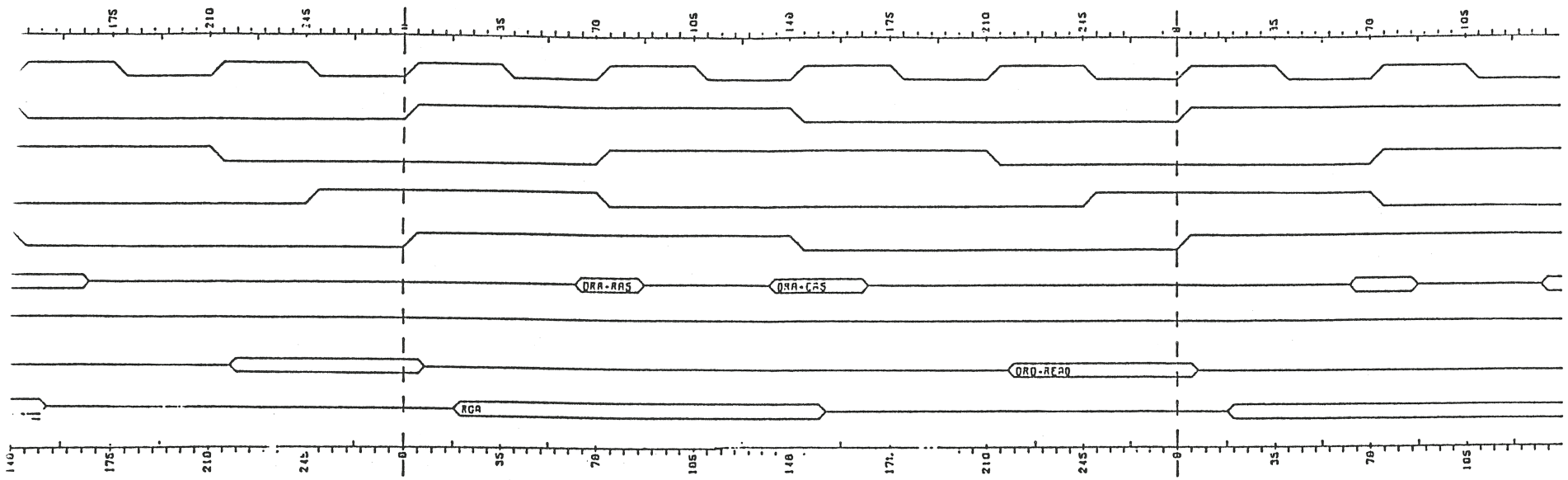
TRADITIONAL REGISTER WRITE CYCLE



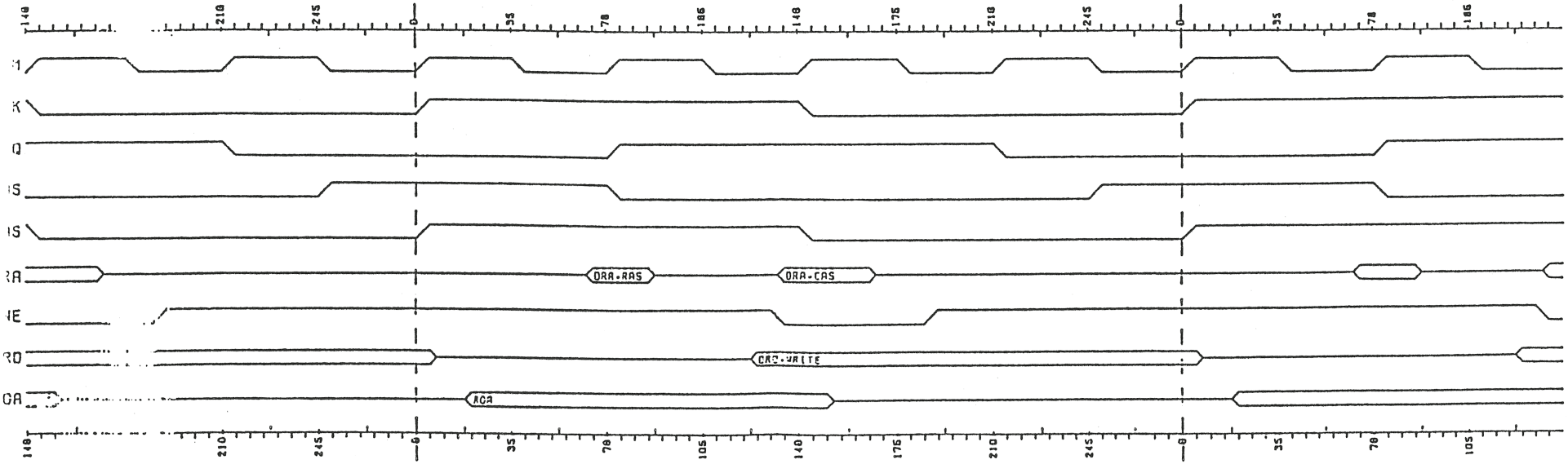
TRADITIONAL RAS-ONLY REFRESH



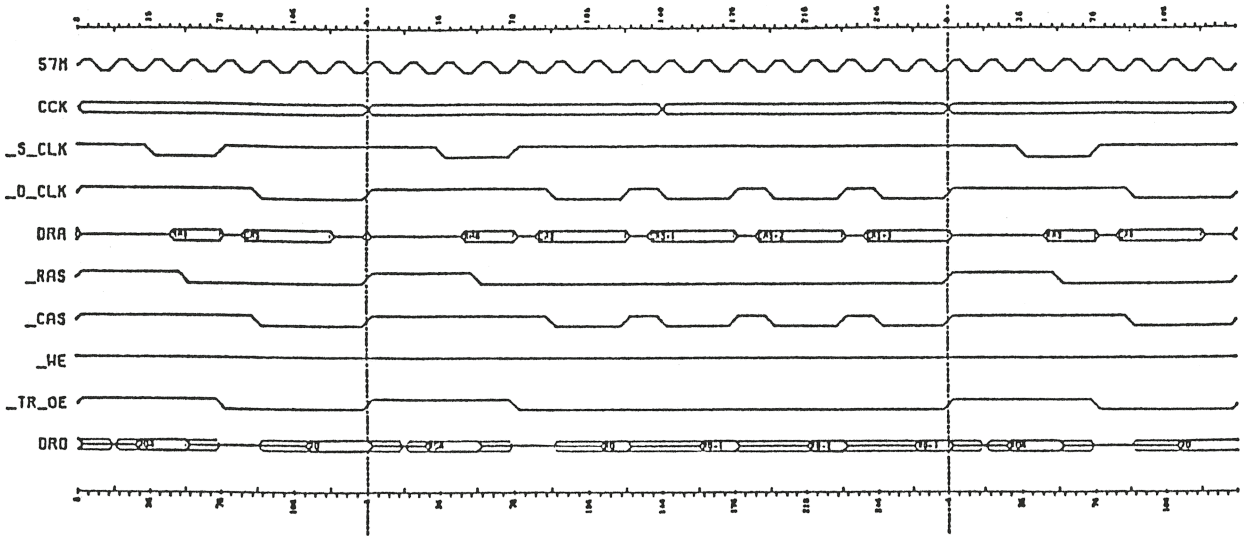
TRADITIONAL NULL CYCLE



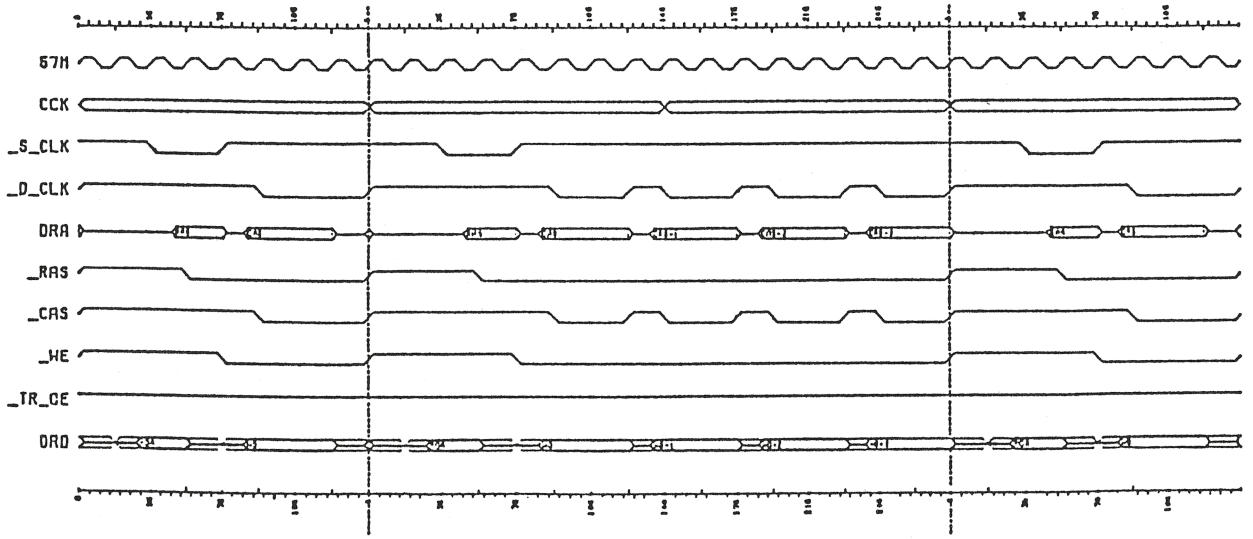
TRADITIONAL DRAM READ CYCLE



TRADITIONAL DRAM WRITE CYCLE

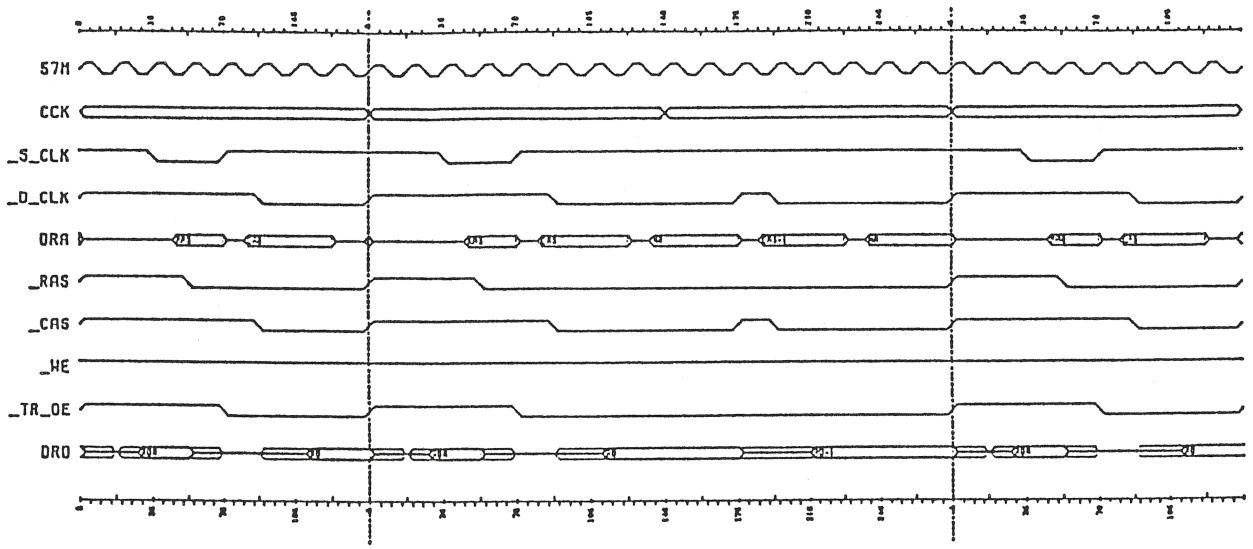


READ CYCLE (QUAD CAS)

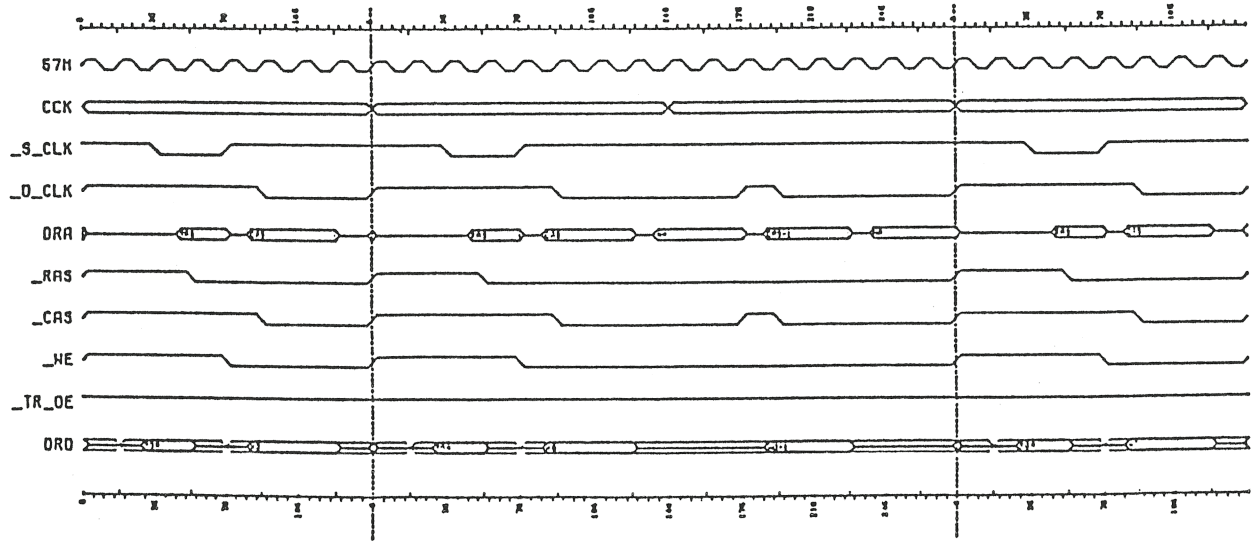


WRITE CYCLE (QUAD CAS)

A+ Chip Bus Timing (Double Speed) 03/31/92

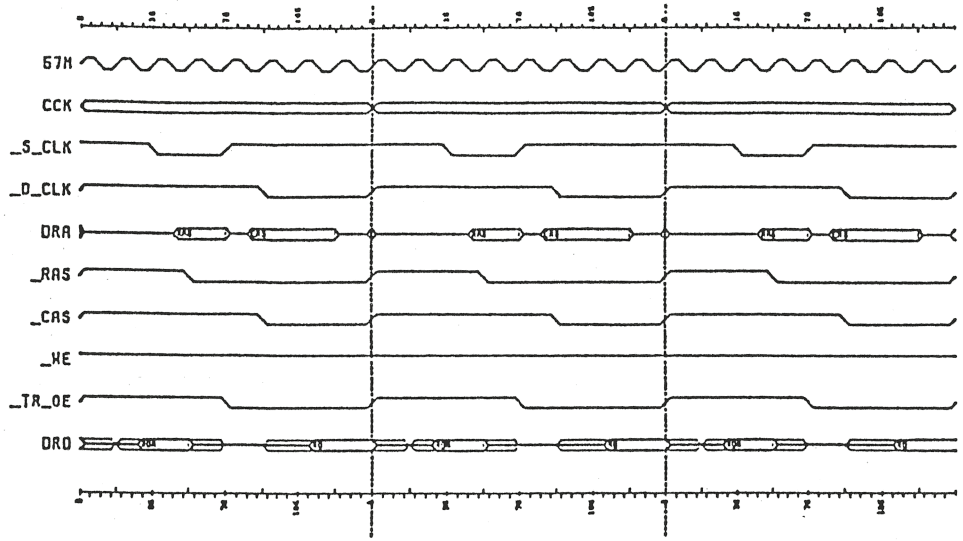


READ CYCLE (DOUBLE CAS)

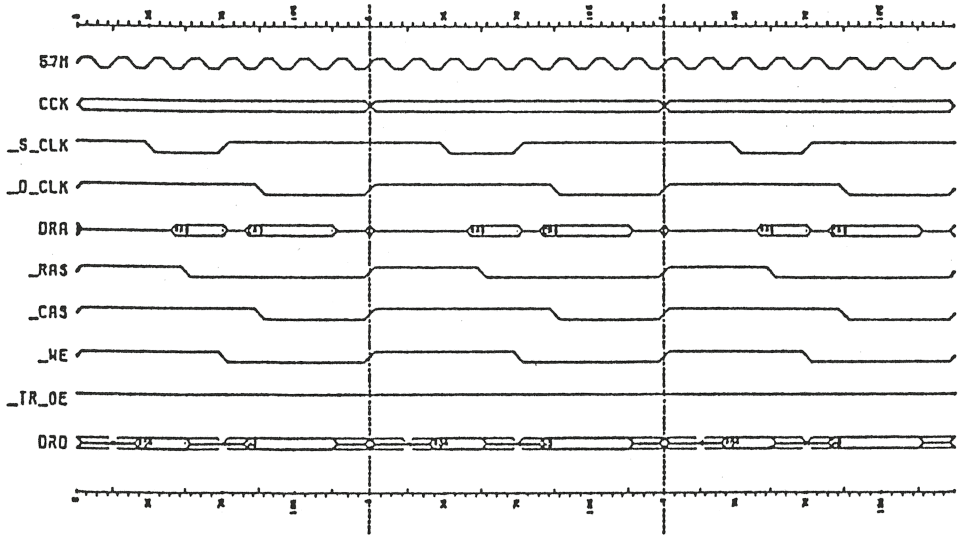


WRITE CYCLE (DOUBLE CAS)

A+ Chip Bus Timing (Double Speed) 03/31/92

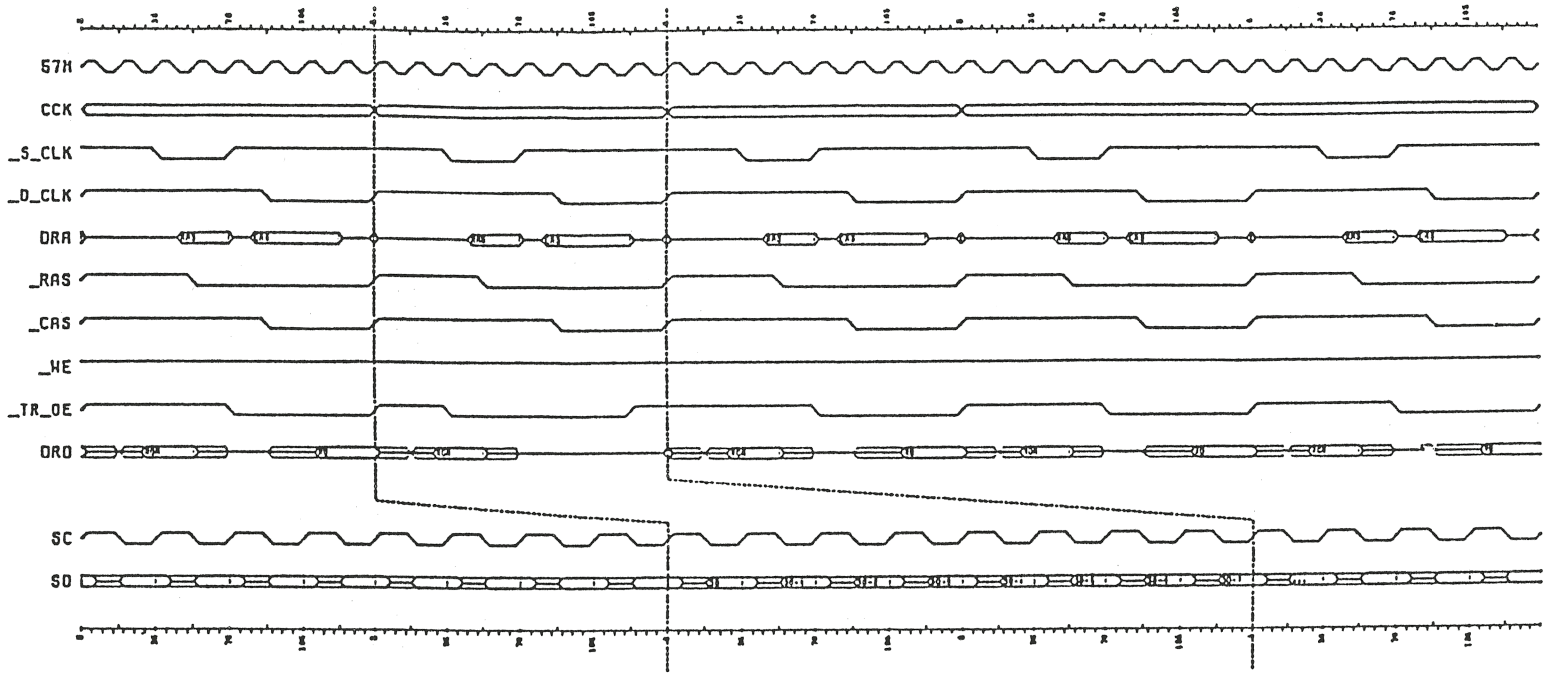


READ CYCLE (SINGLE CAS)

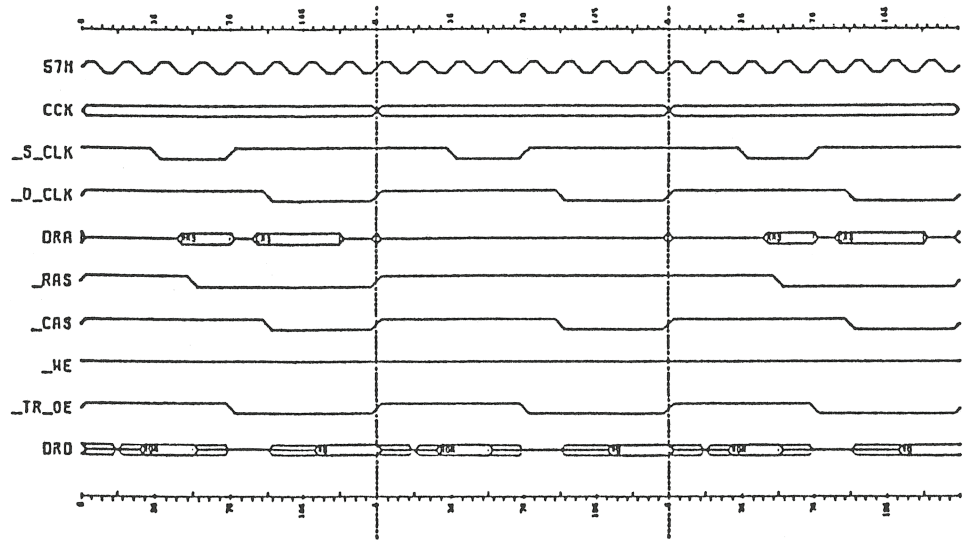


WRITE CYCLE (SINGLE CAS)

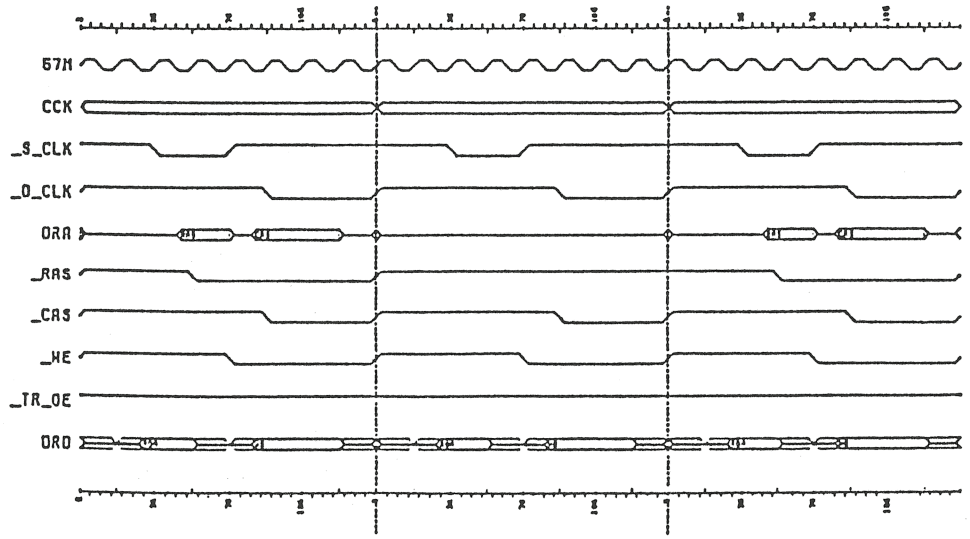
A+ Chip Bus Timing (Double Speed) 03/31/92



SHIFFT REGISTER LOAD CYCLE

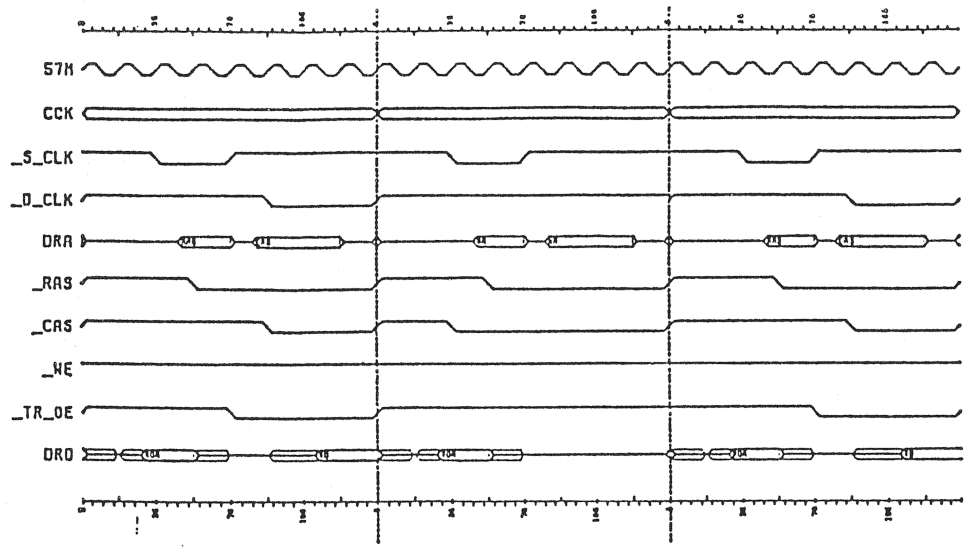


SLOW REGISTER READ

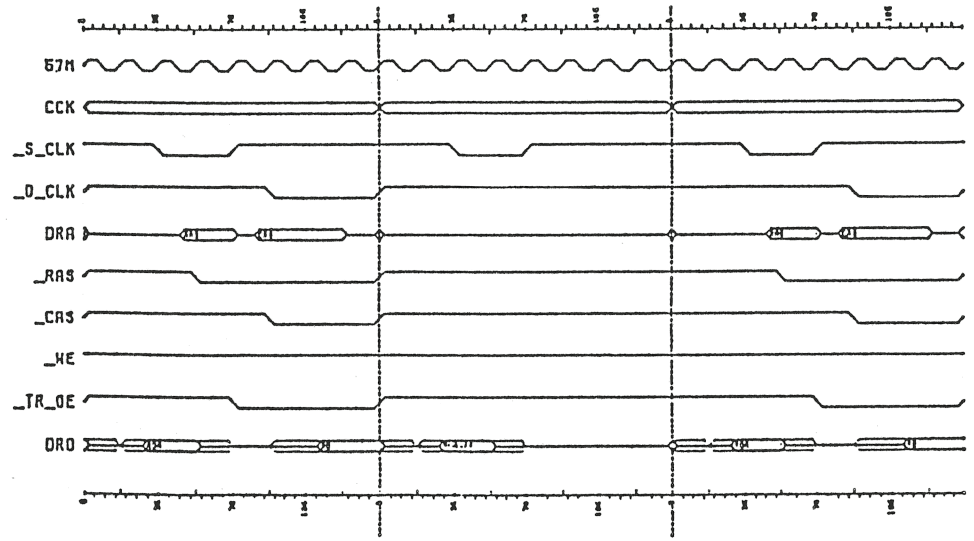


SLOW REGISTER WRITE

Ω+ Chip Bus Timing (Double Speed) 03/31/92

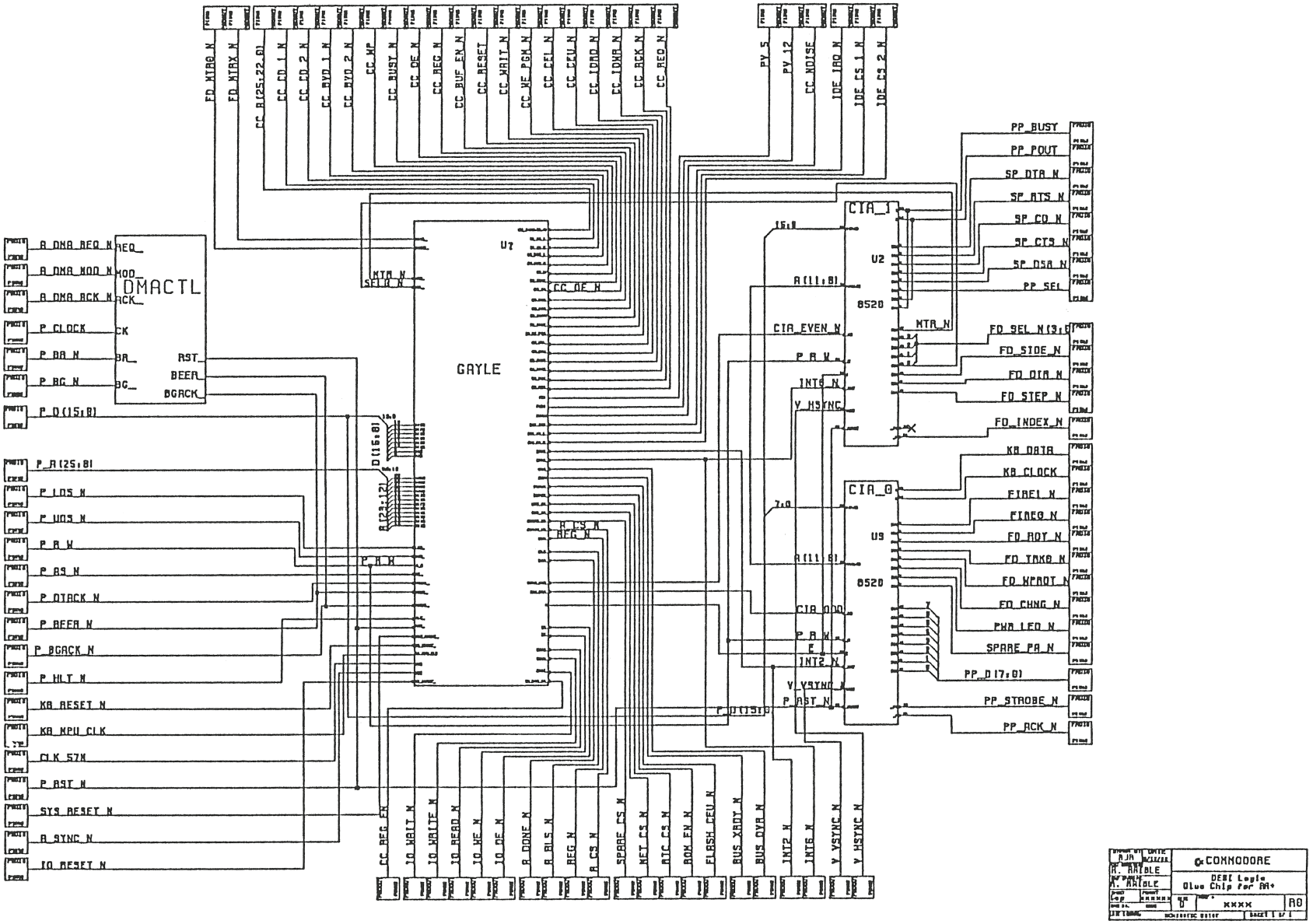


CAS BEFORE RAS REFRESH

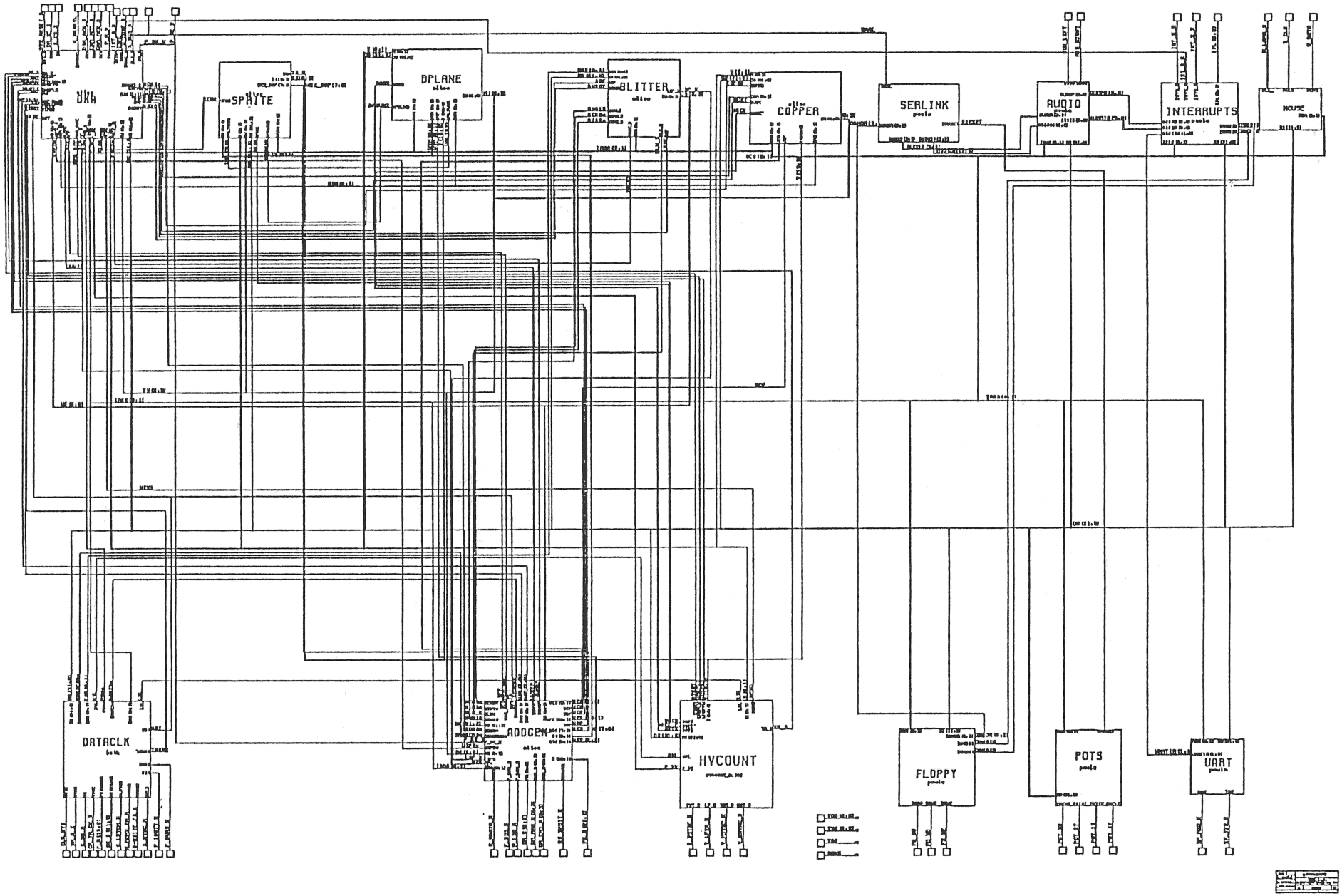


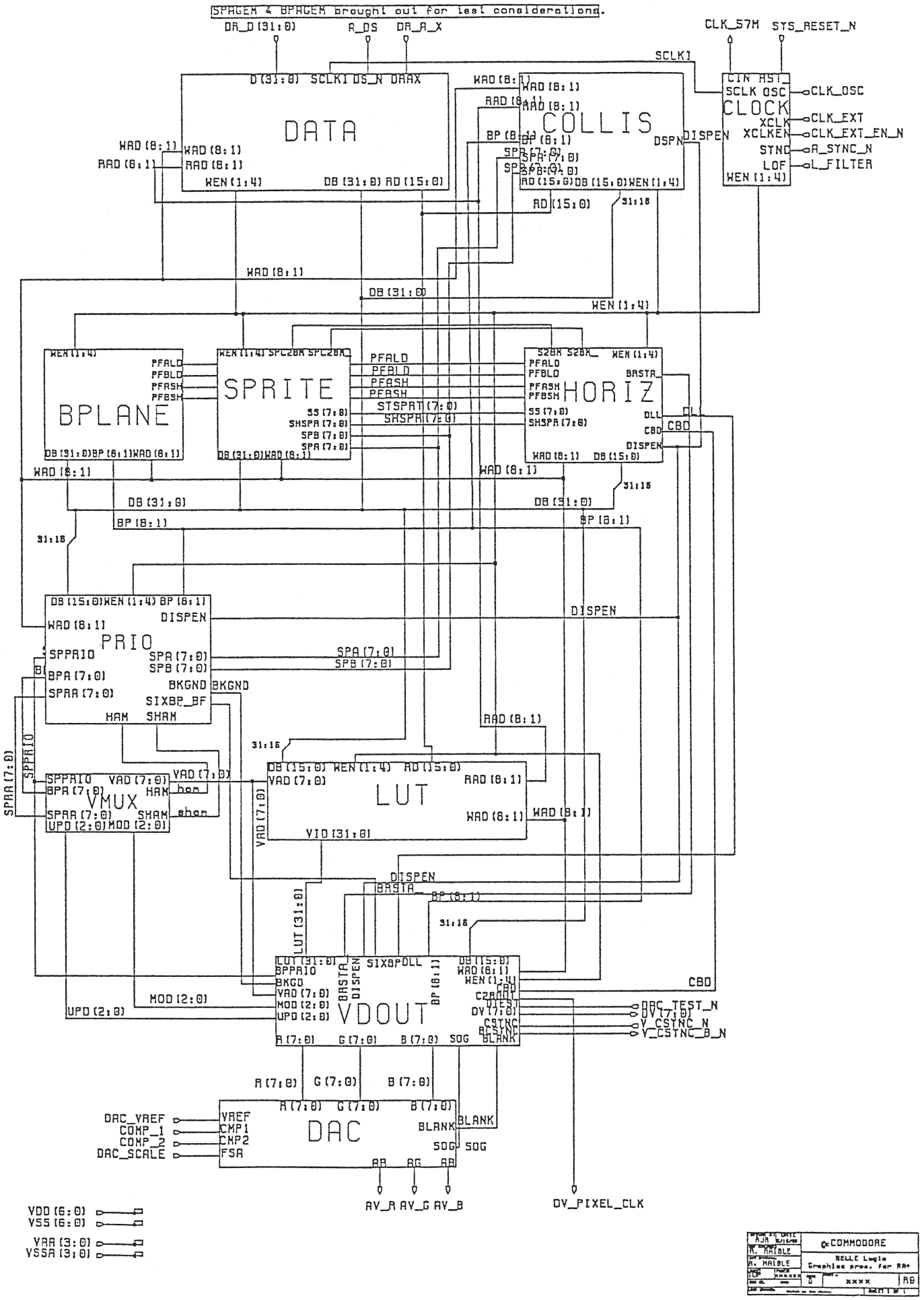
NULL CYCLE

A+ Chip Bus Timing (Double Speed) 03/31/92



AJA		COMMODORE
M. RAIBLE		DESI Logic Blue Chip for A4+
M. RAIBLE		U XXXX R0


DMA
SPRITE
BPLANE
BLITTER
COPPER
SERLINK
AUDIO
INTERRUPTS
MOUSE
DATACLK
ADDGEN
HVCOUNT
FLOPPY
POTS
UART


SPRGEN & BPRGEN brought out for test considerations.
DR_D (31:0)
A_DS
DR_A_X
CLK_57M
SYS_RESET_N
SCLK1
DATA
COLLIS
CLOCK
CLK_OSC
CLK_EXT
XCLKEN
CLK_EXT_EN_N
A_SYNC_N
L_FILTER
BPLANE
SPRITE
HORIZ
PRIO
LUT
VMUX
VDOUT
DAC
DISPEN
CBD
DAC_TEST_N
V_CSYNC_N
V_CSYNC_B_N
DAC_VREF
COMP_1
COMP_2
DAC_SCALE
AV_R
AV_G
AV_B
DV_PIXEL_CLK
VDD (6:0)
VSS (6:0)
VAA (3:0)
VSSA (3:0)
COMMODORE
BELLE Logic
Graphics proc. for AA+